VRFA0127-SG

25.5-27 GHz GaN HPA MMIC

Preliminary Datasheet v3

Features

- Frequency range: 25.5 GHz to 27 GHz
- Saturated power: 11 W
- PAE: 24 %
- Output Power Detector
- Available as bare die or package
- Die dimensions : 3.89 x 3.4 mm
- Package dimensions: 9.76 x 11.71 x 1.91 mm (including leads)
- Package type metal ceramic, hermetic

Description

The VRFA0127-SG is a Ka-band integrated high power amplifier MMIC. The MMIC design is compliant with ECSS-Q-ST-30-11C Rev 1 and is manufactured on a technology successfully evaluated for Space use and referenced in the European Preferred Part List. It is built into a high reliability hermetic metal/ceramic package. It is suitable as an output stage amplifier for applications including payload satellite communications, and able to provide support for variable coding modulation (VCM) modes up to 64-APSK at 37.5 dBm of output power; the amplifier may also be operated in a Beacon mode configuration, by reducing the drain voltage to 8-12 V, depending on user requirements. It is fitted with an output power detector for integration into complex transmission systems.

Electrical characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Drain Voltage (VCM Mode)	V_{D_VCM}		20		V
Quiescent Drain Current (VCM Mode)	I_{DQ_VCM}		1		A
Thermal Resistance Junction-Case	R_{TH_JC}		2.8		°C/W
Hermeticity (typical)		10^{-9} Pa·m^3/s (10^{-8} ccHe/sec.) at 10^5 Pa (1atm) differential			
Temperature (application module baseplate)	T_{BP}	-20	25	50	°C

Note 1: in order to provide a representative operating condition, the temperature used across the datasheet T_{BP} is the temperature measured with a contact thermocouple located under the DUT, within the copper test fixture baseplate. It is estimated that the thermal resistance between the thermocouple and the package case is 0.4°C/W. Please contact VIPER RF for details on the package mount and test fixture configuration.

Note 2: the performance indicated on the datasheet is obtained with a small impedance adjustment on the PCB at the output of the HPA. Please contact VIPER RF for details of the impedance transformation implementation.

Electrical Characteristics

Operating Conditions: VD = 20 V, IDQ = 100 mA/mm (all stages, at 25 °C), T_{BP} = 25 °C

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Frequency Range		Δf	25.5		27	GHz
Small-Signal Gain		S_{21}		27		dB
Power Gain	P_{SAT}	A_{P_PSAT}		14		dB
	1.7 dB back-off	$A_{P\_1.7\_BO}$		17		
	2.9 dB back-off	$A_{P\_2.9\_BO}$		19		
Saturated	P_{SAT}	P_{SAT}		40.5		dBm
VCM Mode RMS Output Power	1.7 dB back-off	$P_{OUT\_1.7\_BO}$		38.8		dBm
	2.9 dB back-off	$P_{OUT\_2.9\_BO}$		37.6		
Power Flatness - Low band	1.7 dB back-off	$\Delta P_{OUT\_LO\_1.7\_BO}$		±0.45		dBm
	2.9 dB back-off	$\Delta P_{OUT\_LO\_2.9\_BO}$		±0.5		
Power Flatness - High band	1.7 dB back-off	$\Delta P_{OUT\_HI\_1.7\_BO}$		±0.3		dBm
	2.9 dB back-off	$\Delta P_{OUT\_HI\_2.9\_BO}$		±0.35		
Output 3rd-Order Intercept Point		OIP3		39.5		dBm
Power-Added	P_{SAT} VCM mode	PAE_{SAT} PAE_{VCM}		24		%
Input Return Loss (dB)		RL_{IN}		-10		dB
Output Return Loss (dB)		RL_{OUT}		-10		

Electrical Characteristics

Operating Conditions: VD = 20 V, IDQ = 100 mA/mm (all stages, set at 25 °C), T_{BP} = 25 °C

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
AM-to-AM	1.7 dB back-off	$AM\text{-}AM_{\_1.7\_BO}$		0.35		dB/dB
	2.9 dB back-off	$AM\text{-}AM_{\_2.9\_BO}$		0.3		
Phase Deviation from Linearity	1.7 dB back-off	$\Delta\Theta_{\_1.7\_BO}$		13		°
	2.9 dB back-off	$\Delta\Theta_{\_2.9\_BO}$		11		
Group Delay Variation, Lo-band	1.7 dB back-off	$\Delta t_{G\_LO\_1.7\_BO}$		70		ps
	2.9 dB back-off	$\Delta t_{G\_LO\_2.9\_BO}$		60		
Group Delay Variation, Hi-band	1.7 dB back-off	$\Delta t_{G\_HI\_1.7\_BO}$		33		ps
	2.9 dB back-off	$\Delta t_{G\_HI\_2.9\_BO}$		26		
Operating Supply Current (VCM mode)		I_D		1.7		A
Die Size			3.89 (W) x 4.3 (H)			mm x mm
Package Dimensions			9.76 x 11.71 x 1.91			mm x mm

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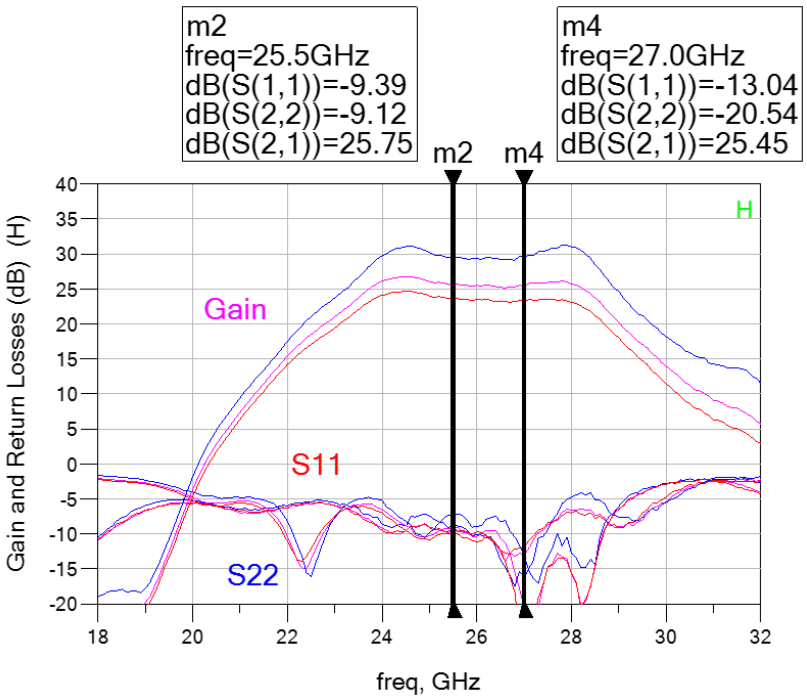
S-Parameters

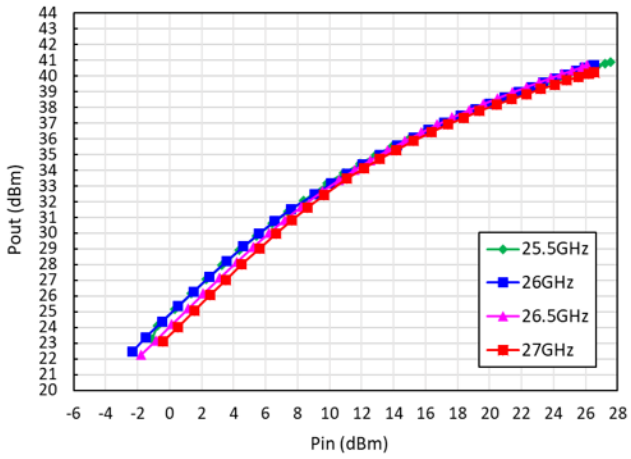
Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = PCB connectors
The total loss of the PCB test fixture is 1.2dB at 27GHz, with return loss better than –16dB.
T_{BP}: Blue = -20°C, Pink = 25°C, Red = 50°C

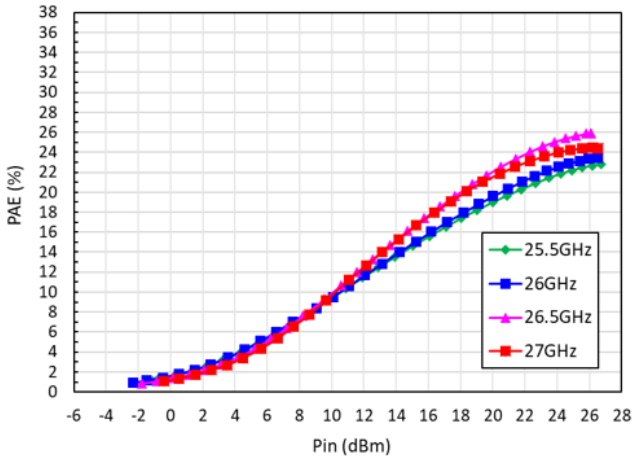


Power and Efficiency Characteristics

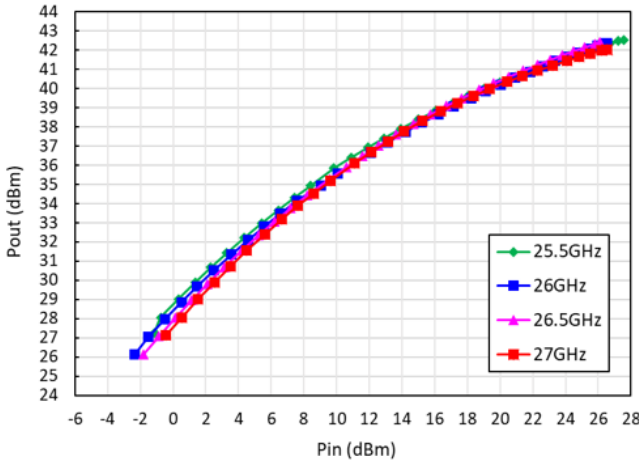
Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

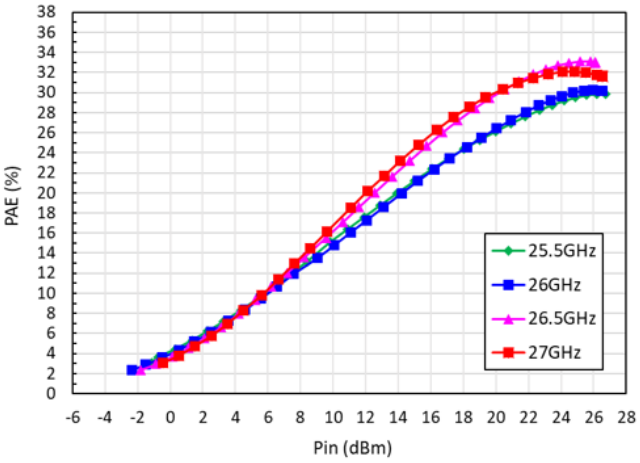
T_{BP} = 25°C:



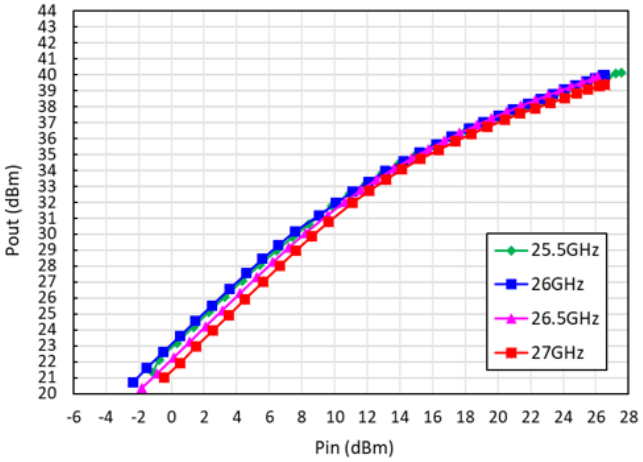


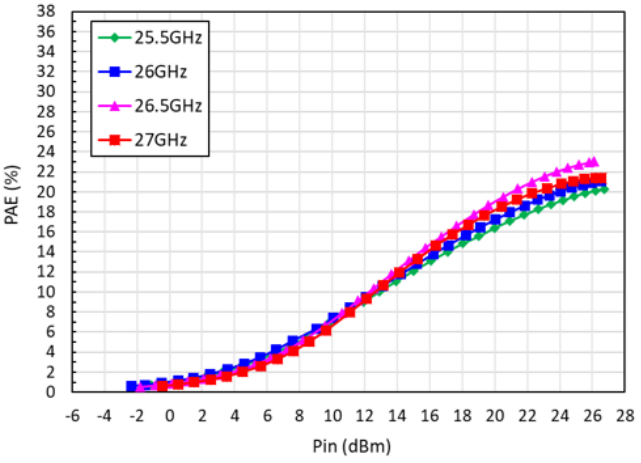
T_{BP} = -20°C:





T_{BP} = 50°C:





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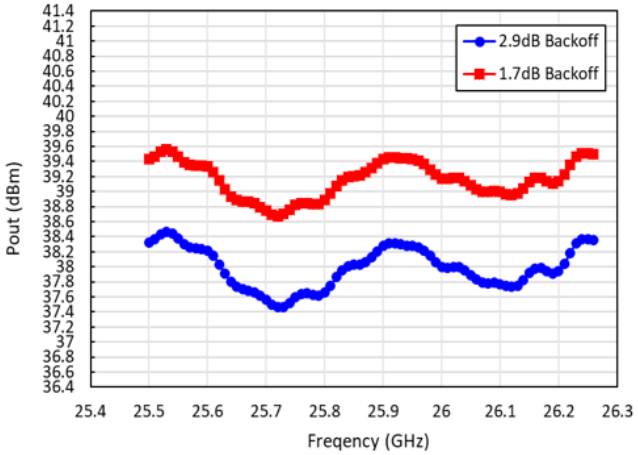
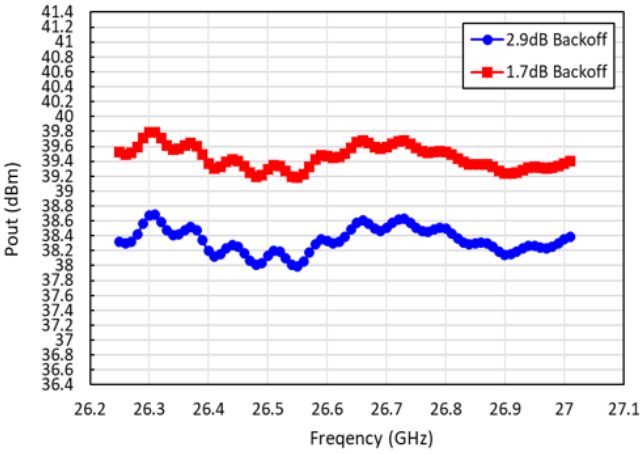
Output Power Flatness Characteristics (per sub-band)

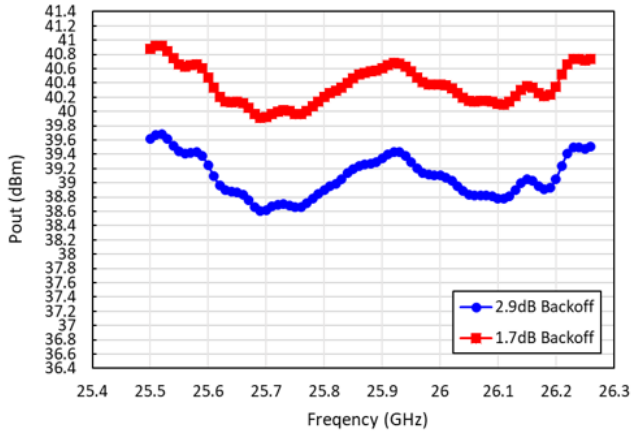
Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

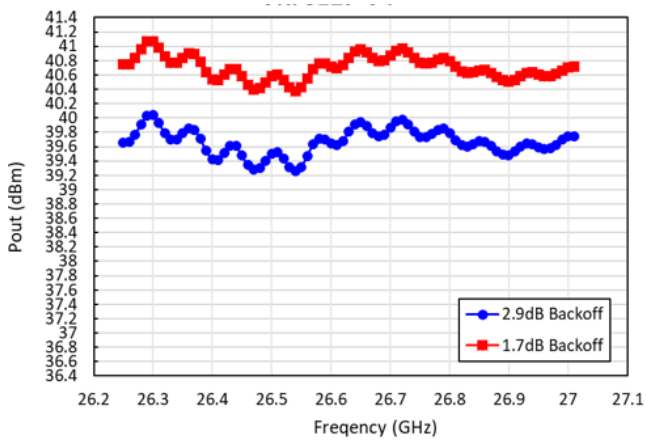
T_{BP} *= 25°C:*



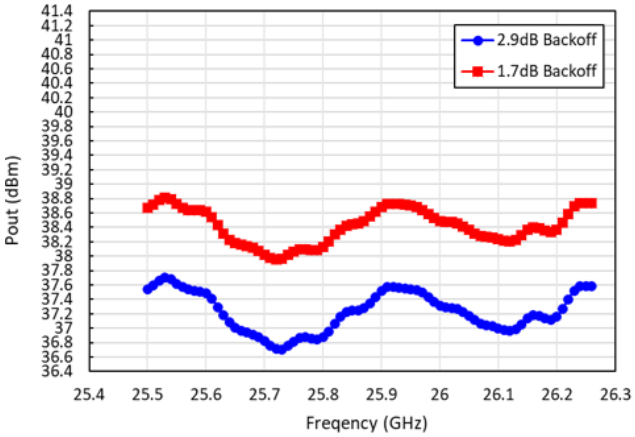


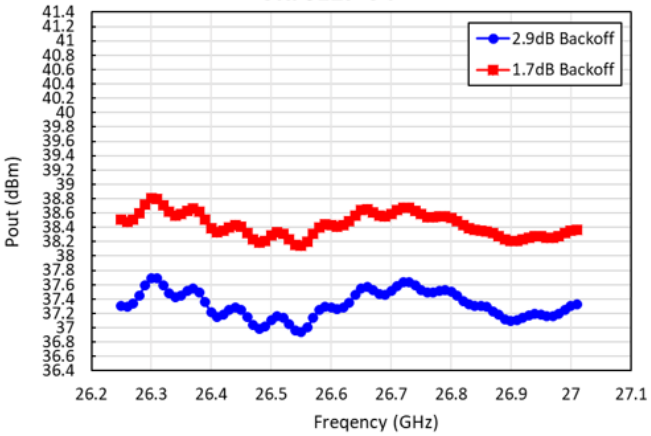
T_{BP} *= -20°C:*





T_{BP} *= 50°C:*





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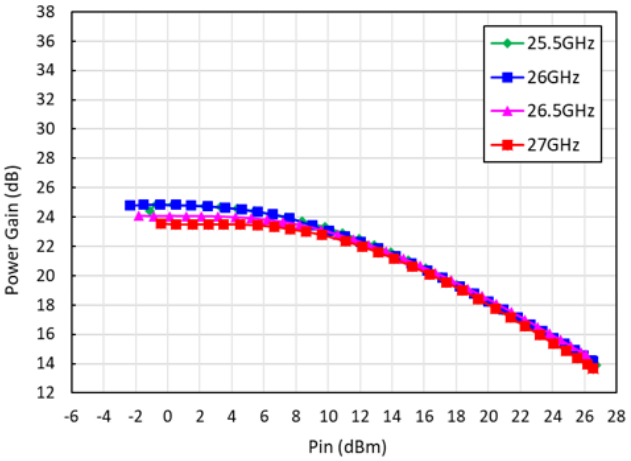
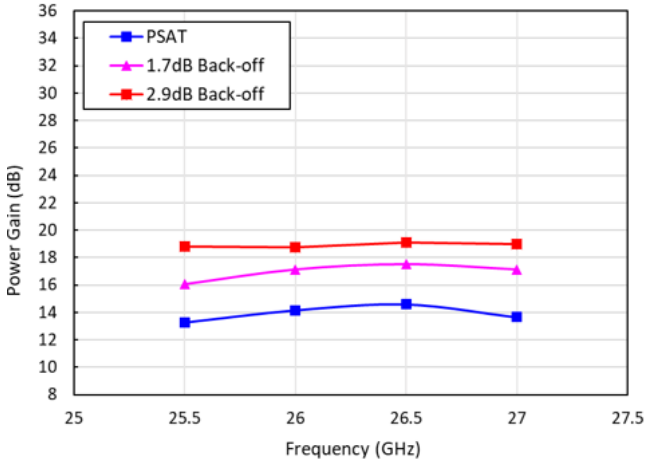
Power Gain Characteristics

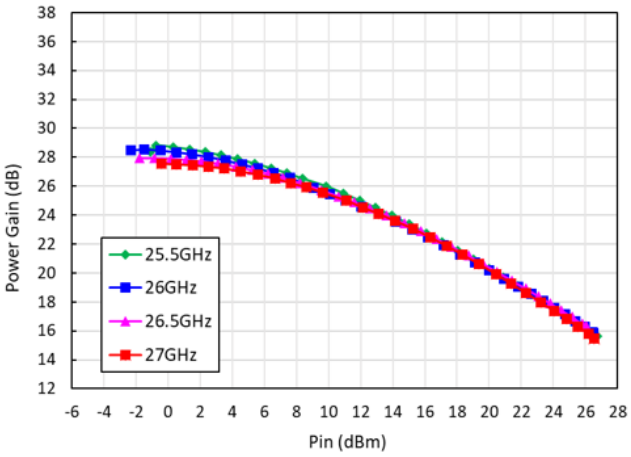
Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

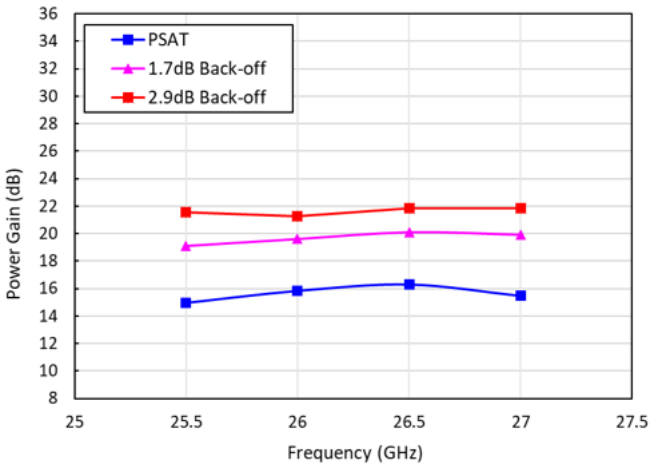
T_{BP} *= 25°C:*



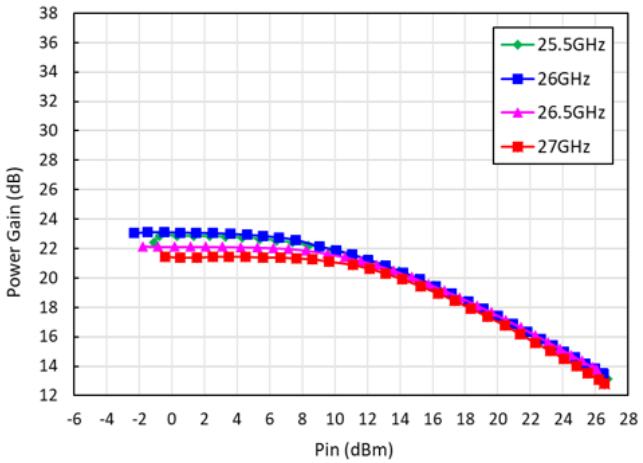


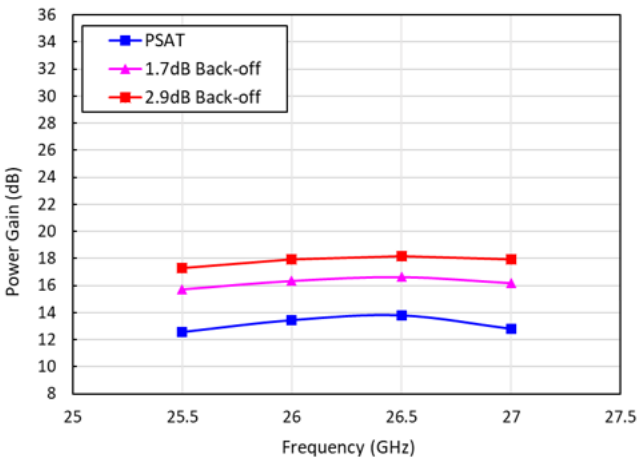
T_{BP} *= -20°C:*





T_{BP} *= 50°C:*





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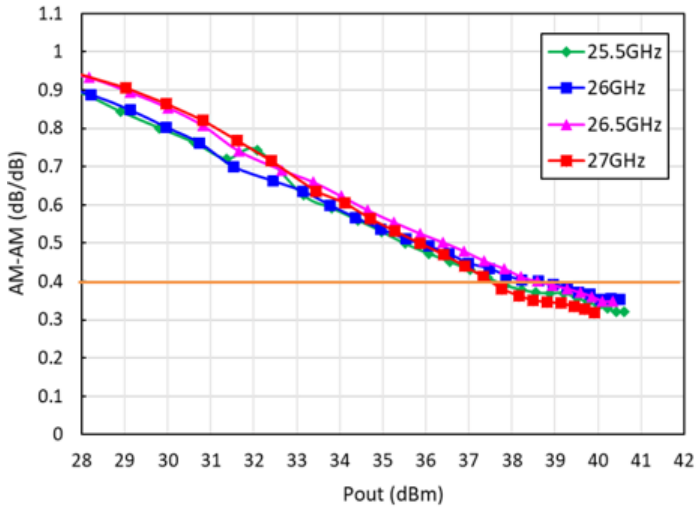
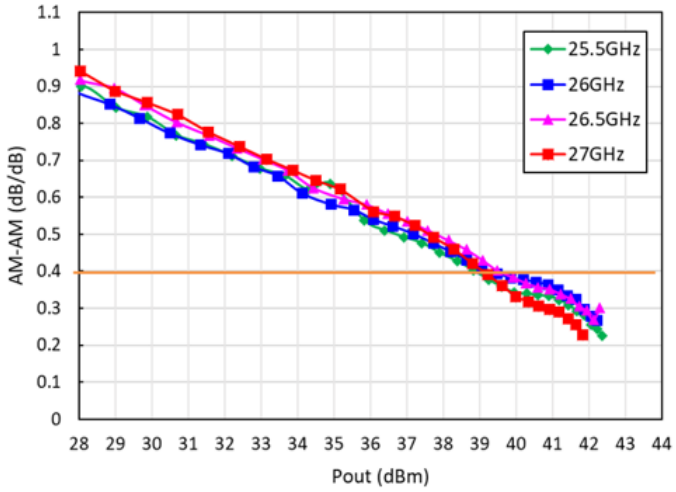
AM-AM Characteristics

Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

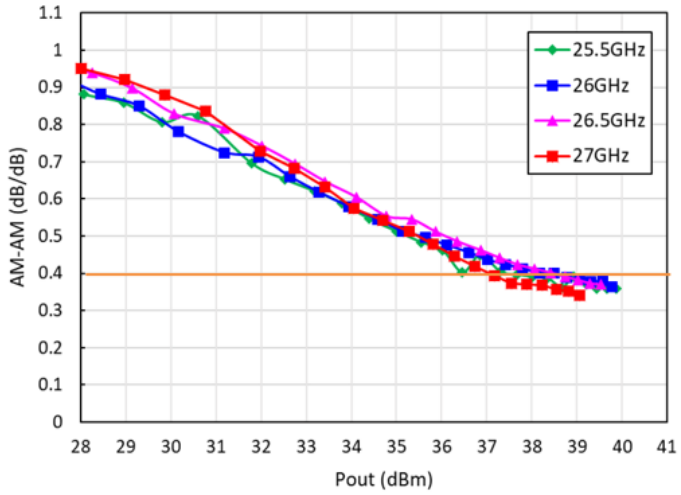
T_{BP} *= 25°C:*



T_{BP} *= -20°C:*



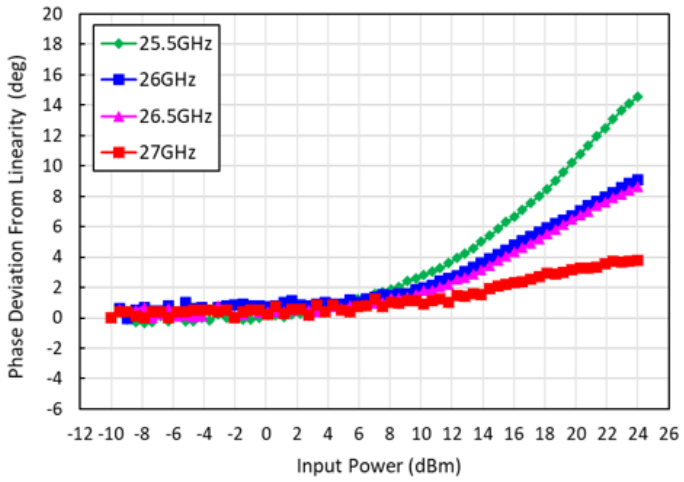
T_{BP} *= 50°C:*



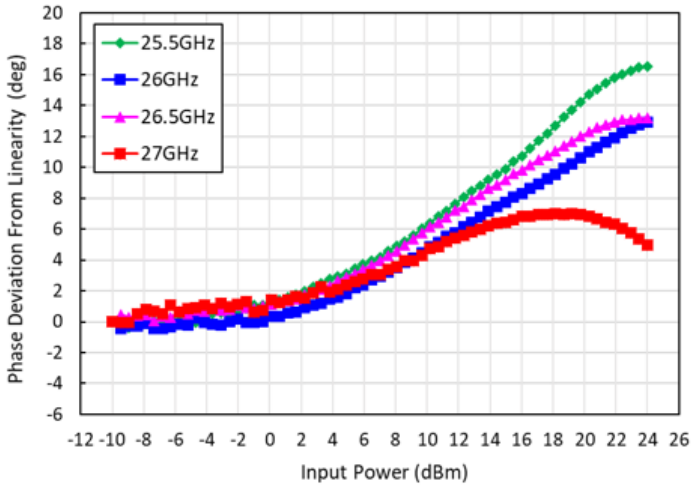
Phase Deviation Characteristics

Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

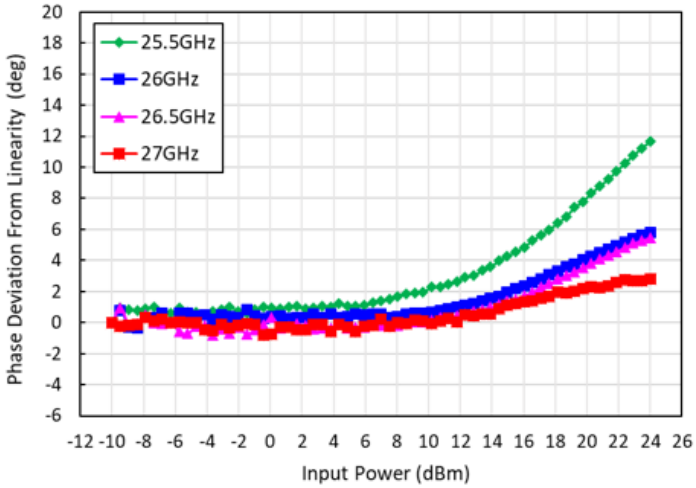
T_{BP} = 25°C:



T_{BP} = -20°C:



T_{BP} = 50°C:



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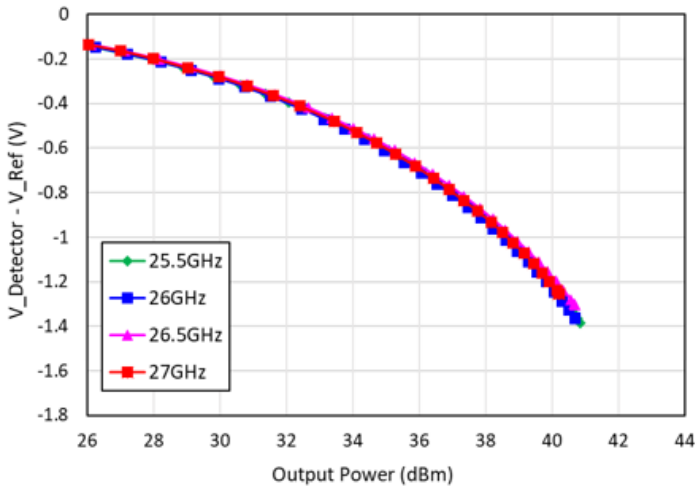
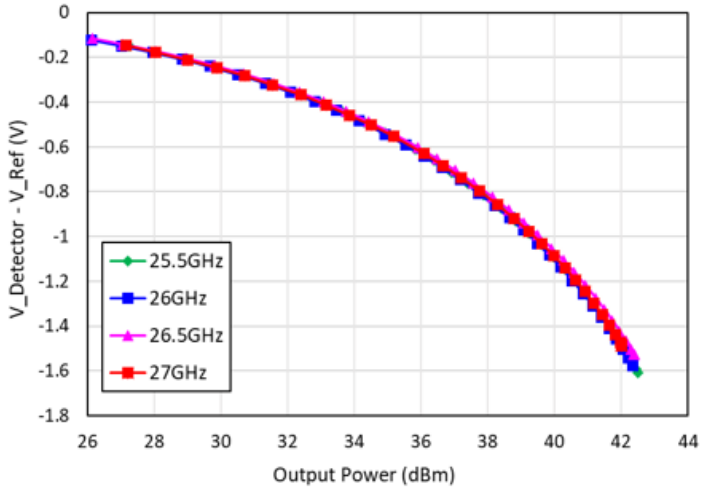
Power Detector Characteristics

Conditions: VD = 20V, IDQ = 1A, VG = -2.85V, Reference plane = Device

T_{BP} = 25°C:



T_{BP} = -20°C:



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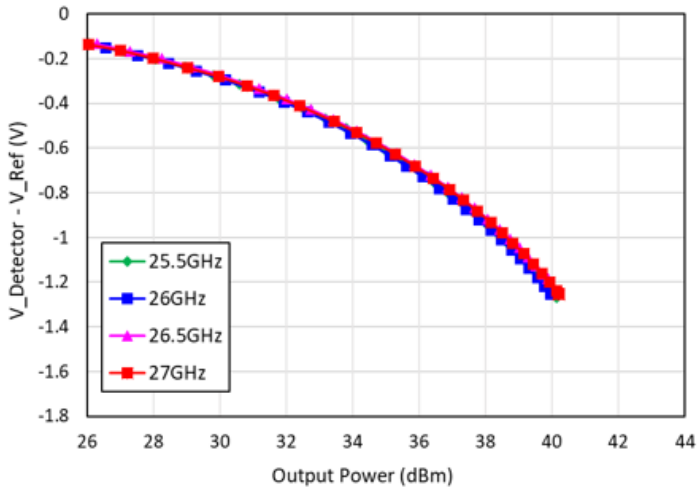

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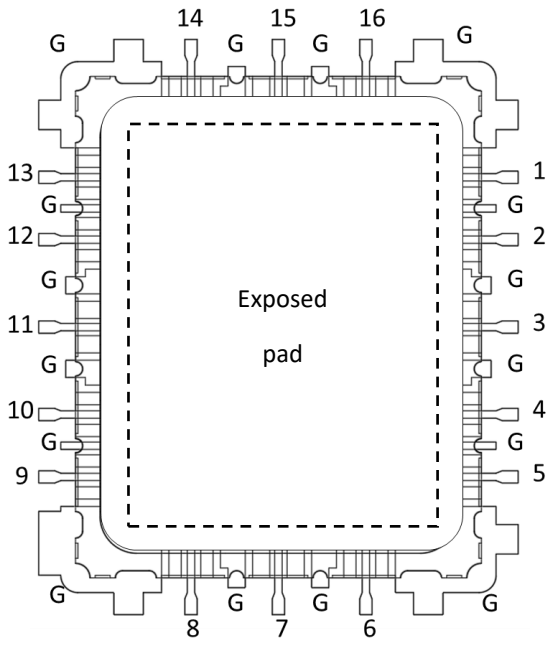
Recommended Absolute Maximum Ratings [1]

Parameter	Symbol	Value	Notes
Drain bias voltage	Vd	27 V	
Minimum gate bias voltage	Vg	-15 V	
Gate Current	Ig	10 mA	
RF input power	RFin	30 dBm 33 dBm	ECSS (50 °C ambient) Commercial (50 °C ambient)
Junction Temperature	T_j	160 °C 200 °C	ECSS Commercial
Storage Temperature	$T_{storage}$	-55 to 150 °C	

[1] Operation outside these conditions may cause permanent damage to the device. Combination of maximum rating conditions may reduce the values. Device performance at these ratings is not implied.

Device Pinout



Pin	Function	Typical DC Operating Voltage (VCM mode)
14, 8	Vg2	-3 to -2.7 V
15, 7	Vd2	20 V
16, 6	Vg3	-3 to -2.7 V
4	Vref	0 to 4.5 V (common mode)
1, 5	Vd3	20 V
2	Vdet	0 to 4.5 V (common mode)
3	RF OUT	DC blocked
9, 13	Vd1	20 V
10, 12	Vg1	-3 to -2.7 V
11	RF IN	DC blocked
G	Ground	
Exposed Pad	Ground	

Note 1: All G pins and features should be connected to the ground net; exposed pad denotes the exposed area under the package, it should also be connected to the ground net and provide a low thermal resistance path. The thermal resistance specified between the transistor junction and the package (table page 1) is referenced to the Exposed Pad.

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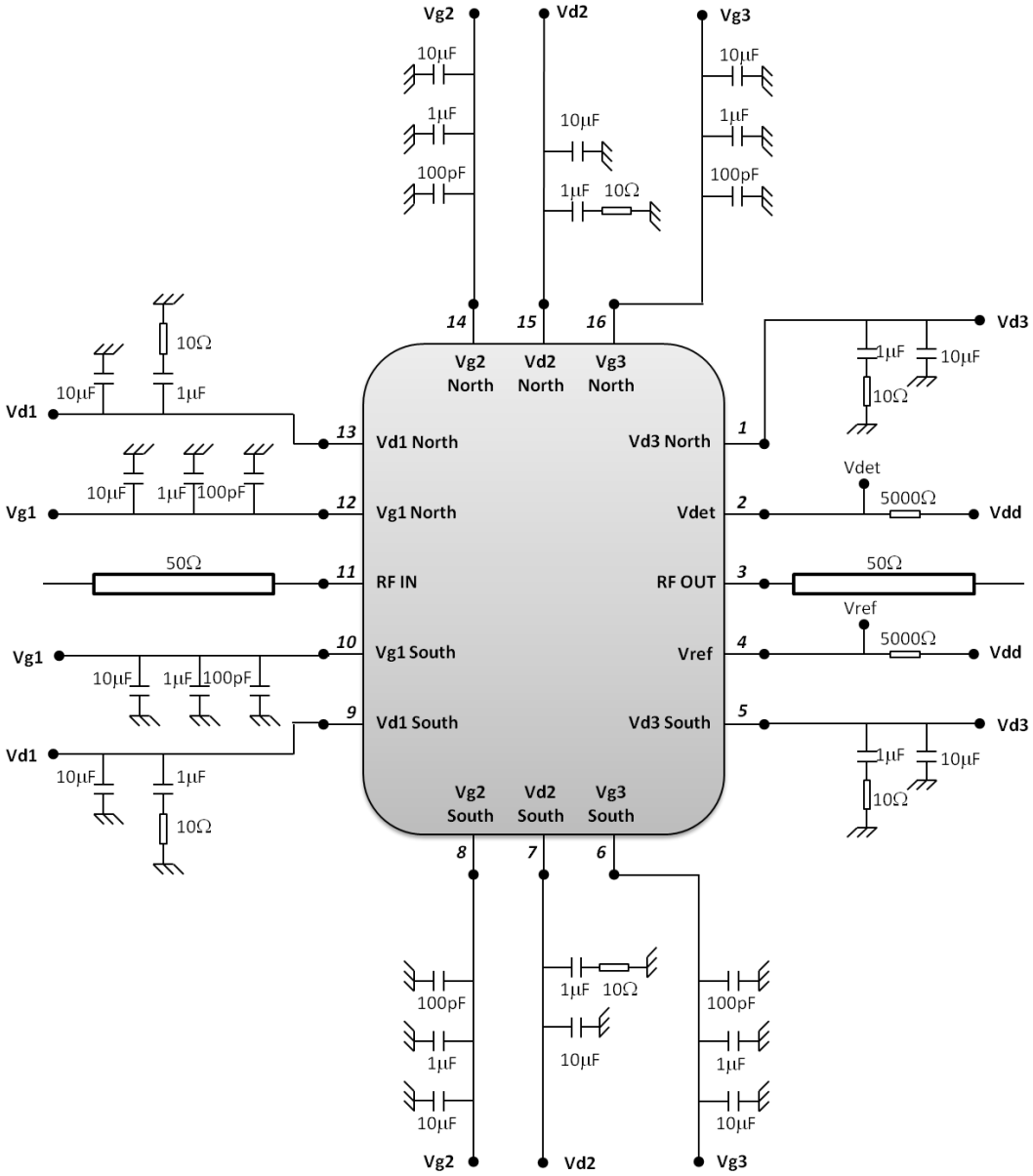
Recommended Application Circuit - Bias Circuits



- *Bias filtering may be amended depending on customer module environment. Please consult the factory if changes are required.*
- *Vref and Vdet are reference and detected voltages, respectively, as a function of output power. The difference of these two voltages can be used for sensing the output power variation. Vdd is a fixed bias voltage equal to typically 4.5V*

Specific Biasing Requirements

- *Nominal bias is obtained by first applying a gate voltage of –2.8V, followed by a drain voltage of 20V (Note sequence). Minor adjustment of the gate voltage may be necessary to obtain the specified quiescent drain current. The RF input signal is applied last.*
- *Sequence for turning off the device is first disabling the RF signal, second the drain voltage, followed by the gate voltage.*

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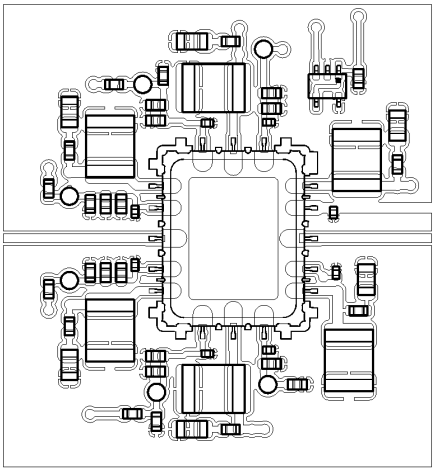
Recommended Application Circuit - PCB Layout

A generic PCB layout for the package is available from VIPER RF. Please consult the factory for the DXF file template. Please note that appropriate heatsinking is required under the exposed pad of the device, such as a coin inserted in the PCB.



Package Information

Package drawing is available from the factory, please consult VIPER RF for further information.

Parameter	Value
Type	Leaded
Body	Al2O3, white
Leads	Fe-Ni-Co Alloy
Lid	Al2O3
Exposed Pad	Cu-Mo alloy
Pin 1	Index mark, circle, Gold
Finish (on leads)	Au plating 0.8µm min Ni plating 2µm to 8µm

Recommended Handling and Assembly

VIPER RF advises the assembly process and reflow profiles should conform to JEDEC J-STD-020.

GaN devices are ESD sensitive and precautions should be observed during storage, handling, assembly and testing.